IN THE SPECIFICATION

Paragraph beginning on page 6, line 26 has been amended as follows:

--In Figs. 4 and 5, reference numeral 8 indicates a conductive material injection-molded over the surfaces of the semiconductor chip 1, 7.--

Paragraph beginning on page 10, line 5 has been amended as follows;

--In Figs. 8 through 10, reference numeral 5 indicates a conductive clip, 5' indicates another conductive clip, 7 indicates one of stacked semiconductor chips, and 7' indicates the other of stacked semiconductor chips. A unit comprising a semiconductor chip 1, 7, surface electrodes 2, 3 or an insulation layer 6, and clip 5 is named as a semiconductor device unit in this embodiment.--

Paragraph beginning on page 11, line 19 has been amended as follows:

--In Figs. 11 through 13, reference numeral 8 indicates a conductive material or conductive layer, and 8' indicates another conductive material or conductive layer. A unit comprising a semiconductor chip 1, 7, surface electrodes 2, 3 or an insulation layer 6, and conductive material 8 is named as a semiconductor device unit in this embodiment.--

Paragraph beginning on page 14, line 8 has been amended as follows:

--Fig. 15 is a sectional view showing a structure of a semiconductor device according to an Eighth Embodiment. A unit comprising a semiconductor chip 7, surface electrodes 2, insulation layer 6, and clip 5 is named as a semiconductor device unit in this embodiment.--

Paragraph beginning on page 14, line 12 has been amended as follows:

--An element of the semiconductor device of this embodiment is the semiconductor device unit described referring to Fig. 3, in which conductive clips 5 clamping the top-surface electrodes 2 and the insulation layers 6 on the back surface are provided on one end of each of the semiconductor chips 7. Each of the semiconductor chips 7 has a conductive pattern 9 on the top surface, and are placed on a packaging board 10 perpendicularly to the packaging board 10, and the conductive clips 5 are electrically connected and fixed to the conductive patterns 9 on the packaging board 10.--

A5

Paragraph beginning on page 14, line 28 and ending on page 15, line 2 has been amended as follows:

-- Alternatively, in the semiconductor device, the semiconductor chips 7 have top-surface electrodes 2 and insulation layers on the back surfaces which are clamped by conductive clips 5. The conductive clips 5 are extended to at least a side of the chips 1 (i.e., top-back connecting terminal or connecting material) are connected and fixed to the packaging board 10. --

A6

Paragraph beginning on page 15, line 3 has been amended as follows:

--By this, semiconductor chips 7 can be placed at a predetermined angle, such as a right angle, against the packaging board 10, and high-density packaging can be performed.--

A7

Paragraph beginning on page 15, line 8 has been amended as follows:

--Fig. 16 is a sectional view showing a structure of a semiconductor device according to a Ninth Embodiment. A unit comprising a semiconductor chip 7, surface electrodes 2, insulation layer 6 and conductive material 8 is named as a semiconductor device unit in this embodiment.--

A8

Paragraph beginning on page 15, line 29 and ending on page 16, line 4 has been amended as follows:

--Alternatively, in the semiconductor device, the back surface of semiconductor chips 7 is insulation-treated, and top-surface electrodes 2 and insulation layers 6 on the back surfaces are connected by injection-molded conductive materials 8, and the conductive materials 8 formed on at least a side of the chips 7 (i.e., top-back connecting terminal or connecting material) are connected to the packaging board 10.--

A9

Paragraph beginning on page 16, line 23 has been amended as follows:

--In the semiconductor device of this embodiment, a plurality of semiconductor chips 7 having electrodes 2 formed on the major surfaces, and a plurality of insulators (spacers) 12 having conductive patterns 11 on the top surfaces are alternately stacked so that the electrodes 2 of the semiconductor chips 7 are electrically connected with the conductive patterns 11 of the insulators (spacers) 12, and the conductive patterns 11 of the insulators (spacers) 12 adjacent to each other are placed so as to be electrically connected to each other.--

A10